

### FEATURES

Easy to Use

Low Cost Solution

Higher Performance than Two or Three Op Amp Design

Unity Gain with No External Resistor

Optional Gains with One External Resistor

(Gain Range 2 to 1000)

Wide Power Supply Range ( $\pm 2.6$  V to  $\pm 15$  V)

Available in 8-Lead PDIP and SOIC

Low Power, 1.5 mA max Supply Current

### GOOD DC PERFORMANCE

0.15% Gain Accuracy ( $G = 1$ )

125  $\mu$ V max Input Offset Voltage

1.0  $\mu$ V/ $^{\circ}$ C max Input Offset Drift

5 nA max Input Bias Current

66 dB min Common-Mode Rejection Ratio ( $G = 1$ )

### NOISE

12 nV/ $\sqrt{\text{Hz}}$  @ 1 kHz Input Voltage Noise

0.60  $\mu$ V p-p Noise (0.1 Hz to 10 Hz,  $G = 10$ )

### EXCELLENT AC CHARACTERISTICS

800 kHz Bandwidth ( $G = 10$ )

10  $\mu$ s Settling Time to 0.1% @  $G = 1$ -100

1.2 V/ $\mu$ s Slew Rate

### APPLICATIONS

Transducer Interface

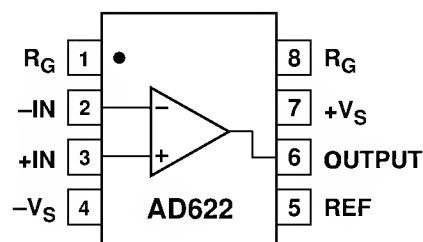
Low Cost Thermocouple Amplifier

Industrial Process Controls

Difference Amplifier

Low Cost Data Acquisition

### CONNECTION DIAGRAM



### PRODUCT DESCRIPTION

The AD 622 is a low cost, moderately accurate instrumentation amplifier that requires only one external resistor to set any gain between 2 and 1,000. Or for a gain of 1, no external resistor is required. The AD 622 is a complete difference or subtracter amplifier "system" while providing superior linearity and common-mode rejection by incorporating precision laser trimmed resistors.

The AD 622 replaces low cost, discrete, two or three op amp instrumentation amplifier designs and offers good common-mode rejection, superior linearity, temperature stability, reliability, and board area consumption. The low cost of the AD 622 eliminates the need to design discrete instrumentation amplifiers to meet stringent cost targets. While providing a lower cost solution, it also provides performance and space improvements.

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
Tel: 617/329-4700 World Wide Web Site: <http://www.analog.com>  
Fax: 617/326-8703 © Analog Devices, Inc., 1997

# AD622- SPECIFICATIONS (typical @ +25°C, $V_S = \pm 15$ V, and $R_L = 2$ k $\Omega$ unless otherwise noted)

Model	Conditions	Min	AD622 Typ	Max	Units
<b>GAIN</b>	$G = 1 + (50.5 \text{ k}/R_G)$				
Gain Range		1		1000	
Gain Error <sup>1</sup>	$V_{OUT} = \pm 10$ V				
$G = 1$			0.05	0.15	%
$G = 10$			0.2	0.50	%
$G = 100$			0.2	0.50	%
$G = 1000$			0.2	0.50	%
Nonlinearity,	$V_{OUT} = \pm 10$ V				
$G = 1$ -1000	$R_L = 10$ k $\Omega$		10		ppm
$G = 1$ -100	$R_L = 2$ k $\Omega$		10		ppm
Gain vs. Temperature	Gain <1000 <sup>1</sup>			-50	ppm/°C
<b>VOLTAGE OFFSET</b>	(Total RTI Error = $V_{OSI} + V_{OSO}/G$ )				
Input Offset, $V_{OSI}$	$V_S = \pm 5$ V to $\pm 15$ V		60	125	$\mu$ V
Average TC	$V_S = \pm 5$ V to $\pm 15$ V			1.0	$\mu$ V/°C
Output Offset, $V_{OSO}$	$V_S = \pm 5$ V to $\pm 15$ V		600	1500	$\mu$ V
Average TC	$V_S = \pm 5$ V to $\pm 15$ V			15	$\mu$ V/°C
Offset Referred to the Input vs. Supply (PSR)	$V_S = \pm 5$ V to $\pm 15$ V				
$G = 1$		80	100		dB
$G = 10$		95	120		dB
$G = 100$		110	140		dB
$G = 1000$		110	140		dB
<b>INPUT CURRENT</b>					
Input Bias Current			2.0	5.0	nA
Average TC			3.0		pA/°C
Input Offset Current			0.7	2.5	nA
Average TC			2.0		pA/°C
<b>INPUT</b>					
Input Impedance					
Differential			10  2		G $\Omega$   pF
Common-Mode			10  2		G $\Omega$   pF
Input Voltage Range <sup>2</sup>	$V_S = \pm 2.6$ V to $\pm 5$ V	$-V_S + 1.9$		$+V_S - 1.2$	V
Over Temperature		$-V_S + 2.1$		$+V_S - 1.3$	V
	$V_S = \pm 5$ V to $\pm 18$ V	$-V_S + 1.9$		$+V_S - 1.4$	V
		$-V_S + 2.1$		$+V_S - 1.4$	V
Over Temperature					
Common-Mode Rejection Ratio DC to 60 Hz with 1 k $\Omega$ Source Imbalance	$V_{CM} = 0$ V to $\pm 10$ V				
$G = 1$		66	78		dB
$G = 10$		86	98		dB
$G = 100$		103	118		dB
$G = 1000$		103	118		dB
<b>OUTPUT</b>					
Output Swing	$R_L = 10$ k $\Omega$ , $V_S = \pm 2.6$ V to $\pm 5$ V	$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature		$-V_S + 1.4$		$+V_S - 1.3$	V
	$V_S = \pm 5$ V to $\pm 18$ V	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature		$-V_S + 1.6$		$+V_S - 1.5$	V
Short Current Circuit			$\pm 18$		mA

Model	Conditions	Min	AD622 Typ	Max	Units
DYNAMIC RESPONSE					
Small Signal -3 dB Bandwidth	10 V Step		1000		kH z
G = 1			800		kH z
G = 10			120		kH z
G = 100			12		kH z
G = 1000			1.2		V/μs
Slew Rate			10		μs
Settling Time to 0.1% G = 1-100					
NOISE					
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{(e_{ni}^2)+(e_{no}/G)^2}$		12		nV/√Hz
Input, Voltage Noise, e <sub>ni</sub>			72		nV/√Hz
Output, Voltage Noise, e <sub>no</sub>					
RTI, 0.1 Hz to 10 Hz	f = 1 kHz				
G = 1			4.0		μV p-p
G = 10			0.6		μV p-p
G = 100-1000			0.3		μV p-p
Current Noise			100		fA/√Hz
0.1 Hz to 10 Hz			10		pA p-p
REFERENCE INPUT					
R <sub>IN</sub>	V <sub>IN+</sub> , V <sub>REF</sub> = 0		20		kΩ
I <sub>IN</sub>			+50	+60	μA
Voltage Range		-V <sub>S</sub> + 1.6		+V <sub>S</sub> - 1.6	V
Gain to Output			1 ± 0.0015		
POWER SUPPLY					
Operating Range <sup>3</sup>	V <sub>S</sub> = ±2.6 V to ±18 V	±2.6		±18	V
Quiescent Current			0.9	1.3	mA
Over Temperature			1.1	1.5	mA
TEMPERATURE RANGE					
For Specified Performance			- 40 to +85		°C

## NOTES

<sup>1</sup>Does not include effects of external resistor  $R_G$ .<sup>2</sup>One input grounded.  $G = 1$ .<sup>3</sup>This is defined as the same supply range that is used to specify PSR.

Specifications subject to change without notice.

# AD622

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage	$\pm 18$ V
Internal Power Dissipation <sup>2</sup>	650 mW
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm 25$ V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (N, R)	$-65^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Operating Temperature Range	
AD622A	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Lead Temperature Range (Soldering 10 seconds)	$+300^{\circ}\text{C}$

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Specification is for device in free air:

8-Pin Plastic Package:  $\theta_{JA} = 95^{\circ}\text{C}/\text{Watt}$

8-Pin SOIC Package:  $\theta_{JA} = 155^{\circ}\text{C}/\text{Watt}$

## ORDERING GUIDE

Model	Temperature Range	Package Option*
AD622AN	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	N-8
AD622AR	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	SO-8
AD622AR-REEL	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	13" Reel
AD622AR-REEL 7	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	7" Reel

\*N = Plastic DIP, SO = Small Outline.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD622 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## Typical Characteristics (@ $+25^{\circ}\text{C}$ , $V_S = \pm 15$ V, $R_L = 2$ k $\Omega$ , unless otherwise noted)

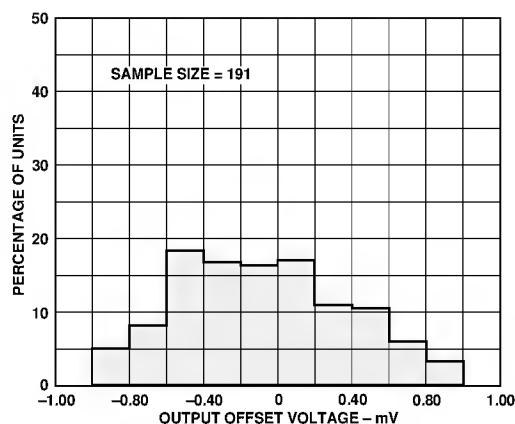


Figure 1. Typical Distribution of Output Offset Voltage

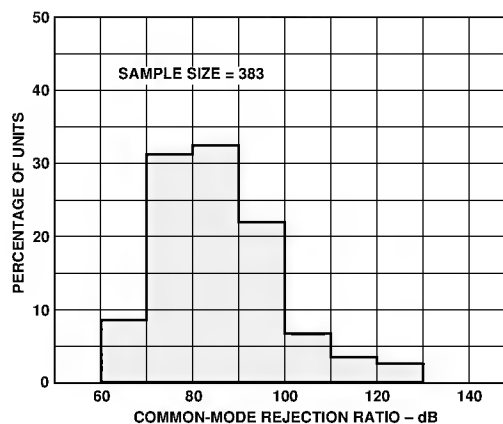


Figure 2. Typical Distribution of Common-Mode Rejection

## Typical Characteristics (@ +25°C, $V_S = \pm 15$ V, $R_L = 2$ k $\Omega$ , unless otherwise noted)

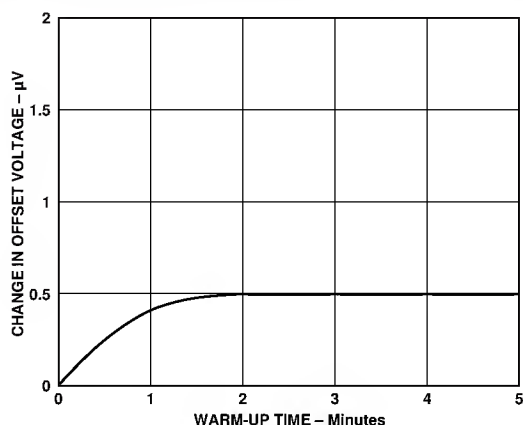


Figure 3. Change in Input Offset Voltage vs. Warm-Up Time

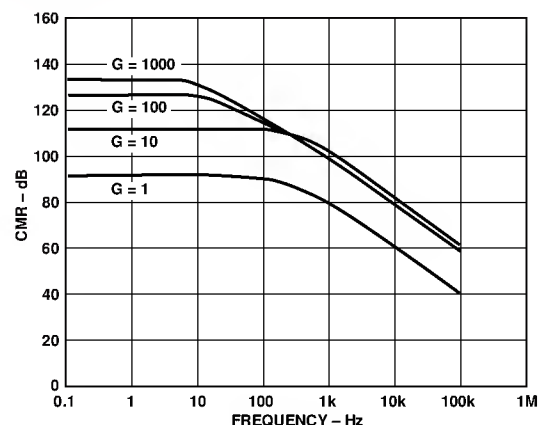


Figure 6. CMR vs. Frequency, RTI, Zero to 1 k $\Omega$  Source Imbalance

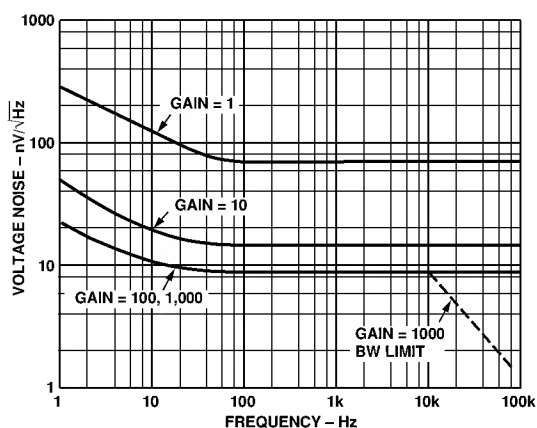


Figure 4. Voltage Noise Spectral Density vs. Frequency, (G = 1-1000)

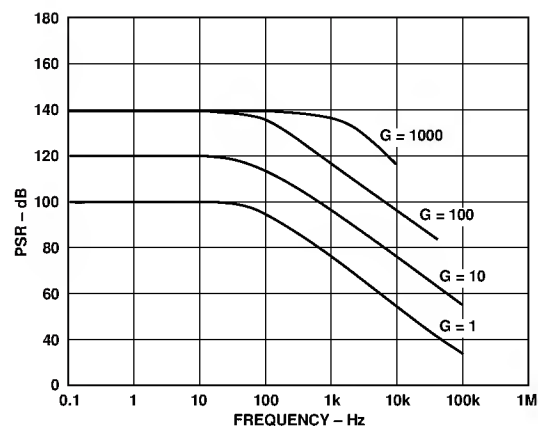


Figure 7a. Positive PSR vs. Frequency, RTI (G = 1-1000)

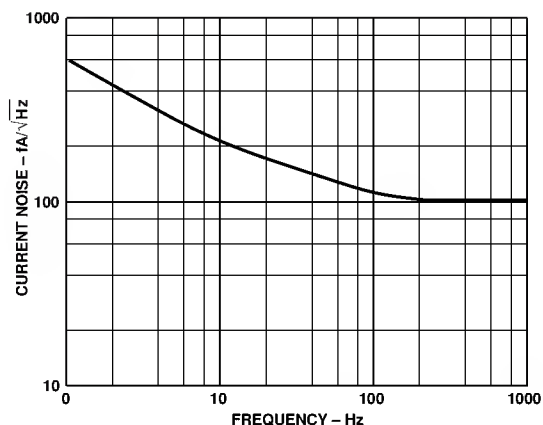


Figure 5. Current Noise Spectral Density vs. Frequency

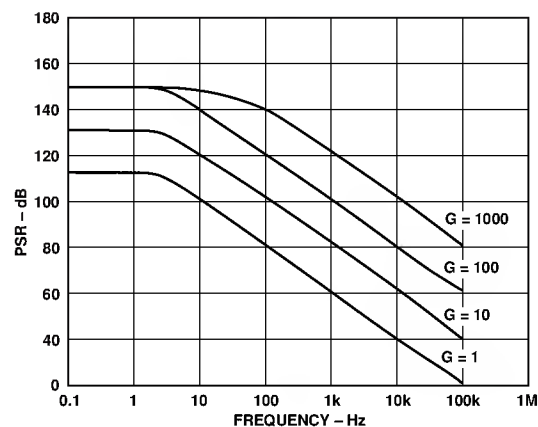


Figure 7b. Negative PSR vs. Frequency, RTI (G = 1-1000)

# AD622- Typical Characteristics (@ +25°C, $V_S = \pm 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , unless otherwise noted)

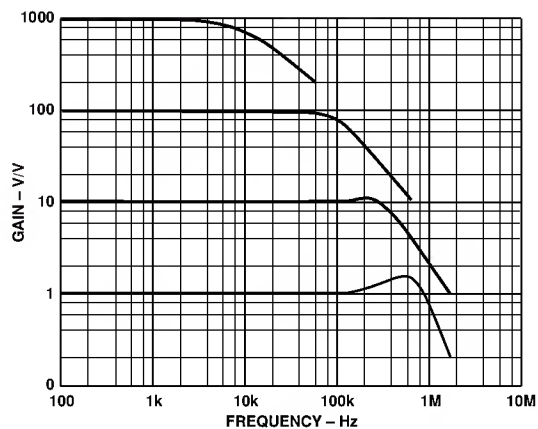


Figure 8. Gain vs. Frequency

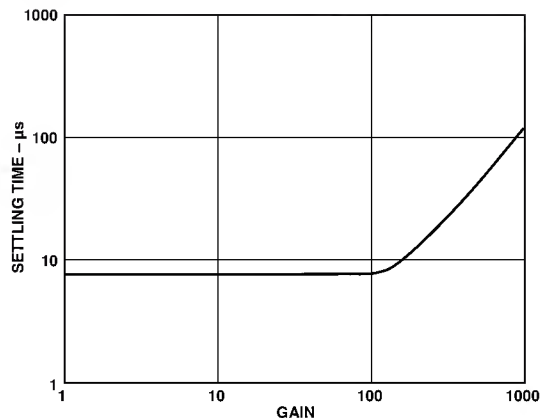


Figure 11. Settling Time to 0.1% vs. Gain, for a 10 V Step

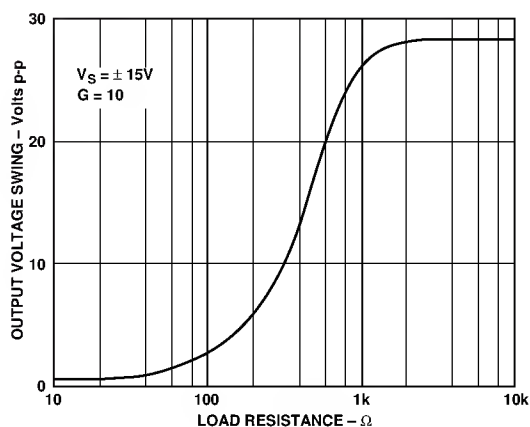


Figure 9. Output Voltage Swing vs. Load Resistance

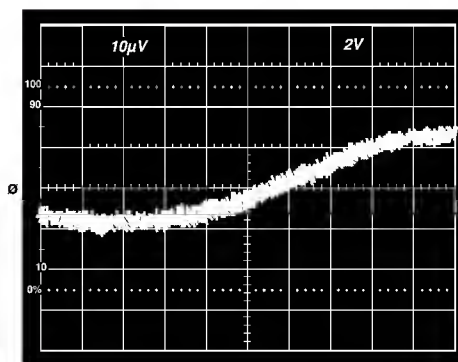


Figure 12. Gain Nonlinearity,  $G = 1$ ,  $R_L = 10\text{ k}\Omega$   
( $20\text{ }\mu\text{V} = 2\text{ ppm}$ )

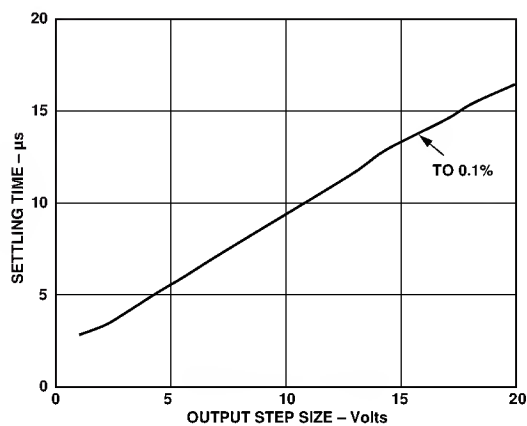


Figure 10. Settling Time vs. Step Size ( $G = 1$ )

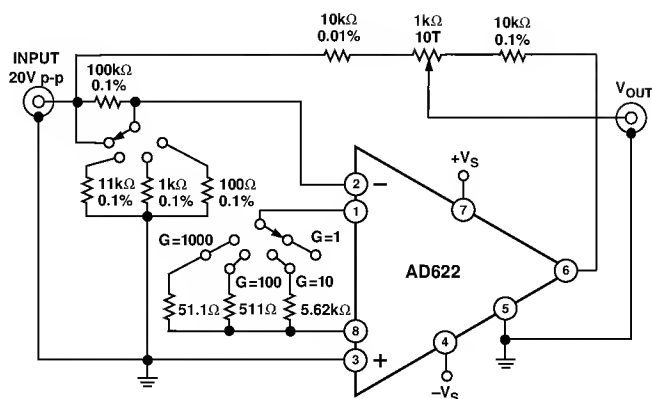


Figure 13. Settling Time Test Circuit

## THEORY OF OPERATION

The AD 622 is a monolithic instrumentation amplifier based on a modification of the classic three op-amp approach. Absolute value trimming allows the user to program gain accurately (to 0.5% at  $G = 100$ ) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus insuring its performance.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain-setting resistor  $R_G$ . This creates a differential gain from the inputs to the A1/A2 outputs given by  $G = (R_1 + R_2)/R_G + 1$ . The unity-gain subtractor A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of  $R_G$  also determines the transconductance of the preamp stage. As  $R_G$  is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 12 nV/ $\sqrt{\text{Hz}}$ , determined mainly by the collector current and base resistance of the input devices.

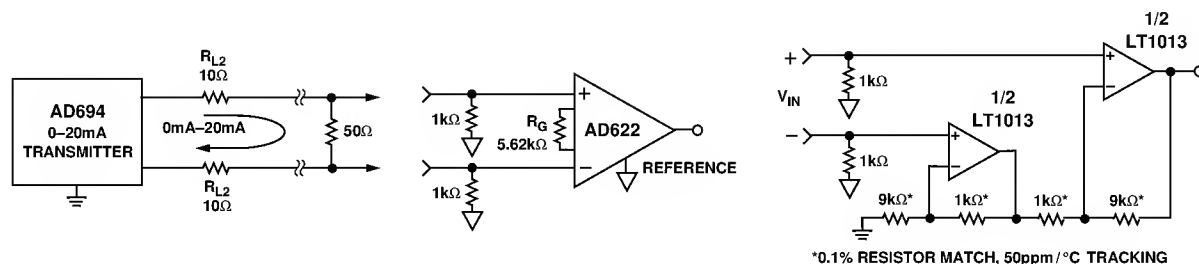
The internal gain resistors, R1 and R2, are trimmed to an absolute value of 25.25 k $\Omega$ , allowing the gain to be programmed accurately with a single external resistor.

## Make vs. Buy: A Typical Application Error Budget

The AD 622 offers a cost and performance advantages over discrete "two op-amp" instrumentation amplifier designs along with smaller size and less components. In a typical application shown in Figure 14, a gain of 10 is required to receive and amplify a 0-20 mA signal from the AD 694 current transmitter. The current is converted to a voltage in a 50  $\Omega$  shunt. In applications where transmission is over long distances, line impedance can be significant so that differential voltage measurement is essential. Where there is no connection between the ground returns of transmitter and receiver, there must be a dc path from each input to ground, implemented in this case using two 1 k $\Omega$  resistors. The error budget detailed in Table I shows how to calculate the effect various error sources have on circuit accuracy.

The AD 622 provides greater accuracy at lower cost. The higher cost of the "homebrew" circuit is dominated in this case by the matched resistor network. One could also realize a "homebrew" design using cheaper discrete resistors which would be either trimmed or hand selected to give high common-mode rejection. This level of common-mode rejection would however degrade significantly over temperature due to the drift mismatch of the discrete resistors.

Note that for the homebrew circuit, the LT 1013 specification for noise has been multiplied by  $\sqrt{2}$ . This is because a "two op-amp" type instrumentation amplifier has two op amps at its inputs, both contributing to the overall noise.



0-20 mA Current Loop  
with 50  $\Omega$  Shunt Impedance

AD622 Monolithic  
Instrumentation Amplifier,  
 $G = 9.986$

"Homebrew" In Amp,  $G = 10$

Figure 14. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD622 Circuit Calculation	"Homebrew" Circuit Calculation	Total Error in ppm Relative to 1 V FS AD622	Total Error in ppm Relative to 1 V FS Homebrew
ABSOLUTE ACCURACY at $T_A = +25^\circ\text{C}$				
Total RTI Offset Voltage, $\mu\text{V}$	$250 \mu\text{V} + 1500 \mu\text{V}/10$	$800 \mu\text{V} \times 2$	400	1600
Input Offset Current, nA	$2.5 \text{ nA} \times 1 \text{ k}\Omega$	$15 \text{ nA} \times 1 \text{ k}\Omega$	2.5	15
CMR, dB	$86 \text{ dB} \rightarrow 50 \text{ ppm} \times 0.5 \text{ V}$	$(0.1\% \text{ Match} \times 0.5 \text{ V})/10 \text{ V}$	25	50
DRIFT TO $+85^\circ\text{C}$		Total Absolute Error	427.5	1665
Gain Drift, ppm/ $^\circ\text{C}$	$(50 \text{ ppm} + 5 \text{ ppm}) \times 60^\circ\text{C}$	$(50 \text{ ppm})/^\circ\text{C} \times 60^\circ\text{C}$	3300	3000
Total RTI Offset Voltage, $\mu\text{V}/^\circ\text{C}$	$(2 \mu\text{V}/^\circ\text{C} + 15 \mu\text{V}/^\circ\text{C}/10) \times 60^\circ\text{C}$	$9 \mu\text{V}/^\circ\text{C} \times 2 \times 60^\circ\text{C}$	210	1080
Input Offset Current, pA/ $^\circ\text{C}$	$2 \text{ pA}/^\circ\text{C} \times 1 \text{ k}\Omega \times 60^\circ\text{C}$	$155 \text{ pA}/^\circ\text{C} \times 1 \text{ k}\Omega \times 60^\circ\text{C}$	0.12	9.3
RESOLUTION		Total Drift Error	3510.12	4089.3
Gain Nonlinearity, ppm of Full Scale	10 ppm	20 ppm	10	20
Typ 0.1 Hz–10 Hz Voltage Noise, $\mu\text{V p-p}$	$0.6 \mu\text{V p-p}$	$0.55 \mu\text{V p-p} \times \sqrt{2}$	0.6	0.778
		Total Resolution Error	10.6	20.778
		Grand Total Error	3948	5575

### GAIN SELECTION

The AD622's gain is resistor programmed by  $R_G$ , or more precisely, by whatever impedance appears between Pins 1 and 8. The AD622 is designed to offer gains as close as possible to popular integer values using standard 1% resistors. Table II shows required values of  $R_G$  for various gains. Note that for  $G = 1$ , the  $R_G$  pins are unconnected ( $R_G = \infty$ ). For any arbitrary gain  $R_G$  can be calculated by using the formula

$$R_G = \frac{50.5 \text{ k}\Omega}{G - 1}$$

To minimize gain error avoid high parasitic resistance in series with  $R_G$ , and to minimize gain drift,  $R_G$  should have a low TC—less than 10 ppm/ $^\circ\text{C}$  for the best performance.

Table II. Required Values of Gain Resistors

Desired Gain	1% Std Table Value of $R_G$ , $\Omega$	Calculated Gain
2	51.1 k	1.988
5	12.7 k	4.976
10	5.62 k	9.986
20	2.67 k	19.91
33	1.58 k	32.96
40	1.3 k	39.85
50	1.02 k	50.50
65	787	65.17
100	511	99.83
200	255	199.0
500	102	496.1
1000	51.1	989.3



### INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD 622 are attributed to two sources, input and output errors. The output error is divided by  $G$  when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total  $V_{OS}$  for a given gain is calculated as:

$$\text{Total Error RTI} = \text{input error} + (\text{output error}/G)$$

$$\text{Total Error RTO} = (\text{input error} \times G) + \text{output error}$$

### REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

### INPUT PROTECTION

The AD 622 features  $400\ \Omega$  of series thin film resistance at its inputs, and will safely withstand input overloads of up to  $\pm 25\text{ V}$  or  $\pm 60\text{ mA}$  for up to an hour. This is true for all gains and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For continuous input overload, the current should not exceed 6 mA ( $I_{IN} \leq V_{IN}/400\ \Omega$ ). For input overloads beyond the supplies, clamping the inputs to the supplies (using a diode such as an 1N 4148) will reduce the required resistance, yielding lower noise.

### RF INTERFERENCE

All instrumentation amplifiers can rectify high frequency out of band signals. Once rectified, these signals appear as dc offset errors at the output. As shown in Figure 15, a low-pass filter can be used to prevent unwanted noise from reaching the differential inputs. A capacitor is connected across the inputs of the instrumentation amplifier and forms a differential low-pass filter with the two resistors. An additional benefit of using a differentially connected capacitor is that it reduces common-mode capacitance imbalance which helps to preserve high frequency common-mode rejection. In applications where the sensor is an RTD or a resistive strain gage, the filter resistors can be omitted if the sensor is physically close to the amplifier inputs. It is important to note that resistor tolerance or mismatch, poor layout and excessive resistor thermal noise (caused by large resistor values) can all contribute to degrading the effectiveness of this filter.

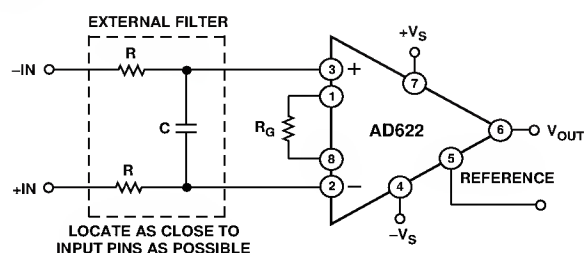


Figure 15. Circuit to Attenuate RF Interference

In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should be properly driven. Figure 16 shows an active guard drive which is configured to improve ac common-mode rejection by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

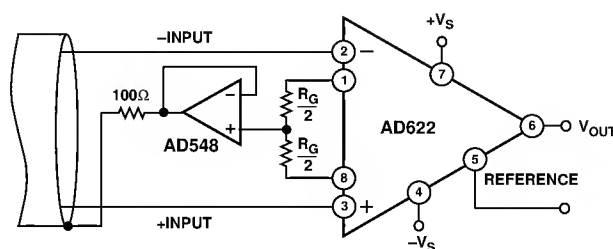


Figure 16. Common-Mode Shield Driver

# AD622

## GROUNDING

Since the AD622 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground." The REF pin should however be tied to a low impedance point for optimal CMR.

The use of ground planes is recommended to minimize the impedance of ground returns (and hence the size of dc errors). In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground returns (Figure 15). All ground pins from mixed signal components such as analog to digital converters should be returned through the "high quality" analog ground plane. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. The digital return currents from the ADC which flow in the analog ground plane will in general have a negligible effect on noise performance.

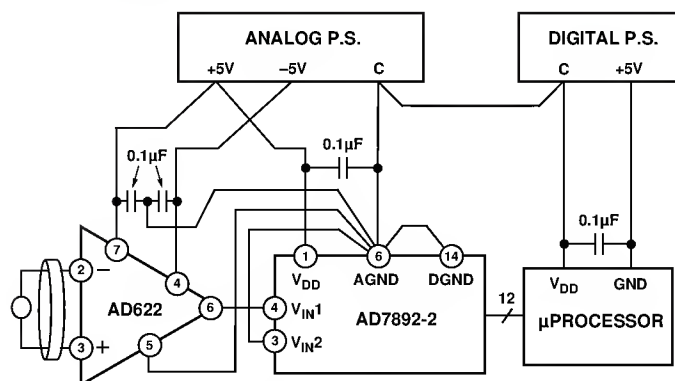


Figure 17. Basic Grounding Practice

## GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 18. Refer to the Instrumentation Amplifier Application Guide (free from Analog Devices) for more information regarding in amp applications.

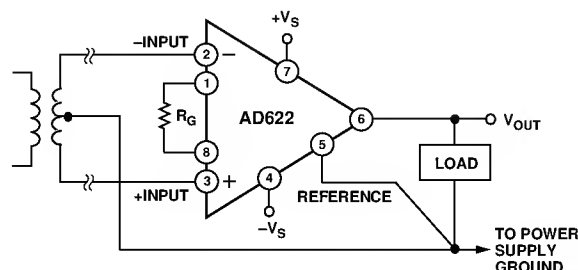


Figure 18a. Ground Returns for Bias Currents with Transformer Coupled Inputs

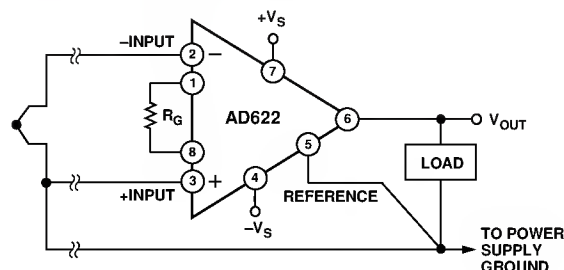


Figure 18b. Ground Returns for Bias Currents with Thermocouple Inputs

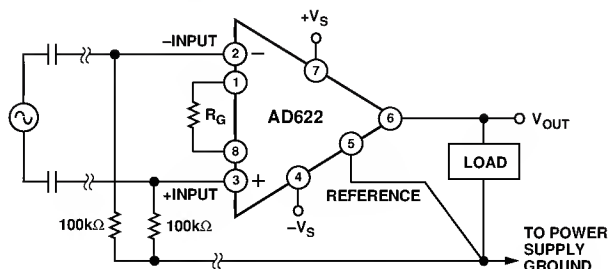
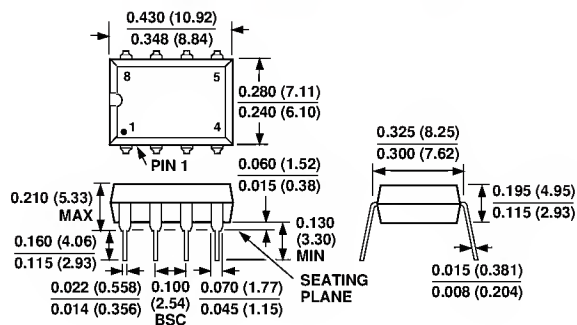


Figure 18c. Ground Returns for Bias Currents with AC Coupled Inputs

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**Plastic DIP (N-8) Package****SOIC (SO-8) Package**